WHAT IS CLAIMED IS:

1. A processor that value predicts for selective instances of read operations, the processor value predicting for those instances of read operations with values that are unavailable in a first memory and requested from a second memory, and that at least partially bases the selective value predictions on accuracy of value predictions for prior corresponding missing instances of the read operations.

2. The processor of claim 1, wherein the first memory includes a low-latency memory.

3. The processor of claim 2, wherein the low-latency memory includes one or more of L1 cache and L2 cache.

4. The processor of claim 1, wherein the second memory includes one or more of L3 cache, random access memory, flash memory, erasable programmable memory, and read-only memory.

5. The processor of claim 1, wherein the processor includes a memory operations unit that comprises a missing read operation value prediction structure used by the processor to value predict for the missing instances of read operations.

6. The processor of claim 5, wherein the memory operations unit includes a load store queue or a memory disambiguation buffer.

7. The processor of claim 5, wherein the missing read operation value prediction structure includes entries to host indications of read operations, predicted values, and value prediction qualifiers.

8. The processor of claim 7, wherein the value prediction qualifiers reflect the accuracy of prior value predictions.

9. The processor of claim 7, wherein the value prediction qualifiers include one or more of confidence values and strength values.

10. The processor of claim 1, wherein the processor causes invocation of a value prediction state machine to value predict for missing instances of read operations, said invocation being coincident with detection of a read operation instance missing in the first memory.

11. The processor of claim 10, wherein the value prediction state machine accesses a missing read operations value prediction encoding to value predict, wherein the first memory hosts at least a part of the missing read operations value prediction encoding.

12. The processor of claim 11, wherein said value prediction state machine accesses the missing read operations value prediction encoding with an address constructed from a base register and from read operation identifying information.

13. The processor of claim 10, wherein the processor causes traps to be issued coincident with arrival of actual values for missing instances of read operations, and a trap handler updates the missing read operations value prediction encoding in accordance with the traps, wherein the issued traps indicate the actual values.

14. The processor of claim 10, wherein the value prediction state machine updates the missing read operations value prediction encoding coincident with arrival of actual values for missing instances of read operations indicated in the missing read operations value prediction encoding.

15. The processor of claim 1, wherein the processor causes traps to be issued coincident with detection of read operation instances missing in the first memory, and a trap handler accesses a missing read operations value prediction encoding to value predict in accordance with the issued traps, wherein the traps at least indicate the missing instances of the read operations.

16. The processor of claim 15, further comprising the trap handler to construct an address to access the missing read operations value prediction encoding.

17. The processor of claim 16, wherein the address is constructed from a base address and read operation identifying information.

18. The processor of claim 15, wherein the first memory hosts at least a part of the missing read operations value prediction encoding.

19. The processor of claim 15, wherein the processor causes traps to be issued coincident with arrival of actual values for value predicted missing instances of read operations, and the trap handler updates the missing read operations value prediction encoding accordingly, wherein the traps coincident with actual value arrivals at least indicate the actual values.

20. The processor of claim 1 further comprising the processor preserving execution state.

21. The processor of claim 20, wherein said preserving execution state comprises checkpointing register state prior to speculative execution of missing instances of read operations with predicted values, and returning to the checkpointed register state for those value predicted missing instances of read operations determined to be mis-predictions.

22. The processor of claim 20, wherein preserving execution state comprises the processor buffering results of instances of operations that are dependent on value predicted instances of read operations, and causing those buffered results that correspond to verified value predicted instances of read operations to be committed.

23. The processor of claim 22, wherein the dependent instances of operations are instances of write operations.

24. The processor of claim 23, wherein the processor includes a first store to host instances of write operations and a second store to host the buffered results of those instances of the write operations that are dependent on missing instances of read operations.

25. A method comprising:

detecting a first instance of a read operation missing in a first memory;

indicating the read operation;

indicating an actual value for the first instance of the read operation, wherein the actual value is from a second memory;

detecting a subsequent instance of the read operation missing in the first memory; and

supplying the indicated value for the read operation's subsequent instance, wherein the indicated value is supplied based, at least in part, on the first and subsequent instances missing in the first memory.

26. The method of claim 25, wherein the first memory includes a low-latency memory.

27. The method of claim 26, wherein the low-latency memory includes one or more of L1 cache and L2 cache.

28. The method of claim 25, wherein the second memory includes one or more of L3 cache, random access memory, flash memory, erasable programmable memory, or read-only memory.

29. The method of claim 25 further comprising:

preserving execution state; and

recovering execution state if the supplied indicated value does not match an actual value determined for the read operation's subsequent instance.

30. The method of claim 29, wherein preserving execution state comprises checkpointing register state.

31. The method of claim 29, wherein preserving execution state comprises buffering results of instances of operations dependent on the subsequent instance of the read operation.

32. The method of claim 31 further comprising committing the buffered results if the supplied indicated value matches the determined actual value.

33. The method of claim 25, wherein the read operation and the actual value for the first instance of the read operation are indicated in a missing read operations value prediction encoding.

34. The method of claim 33, wherein the missing read operations value prediction encoding also indicates a value prediction qualifier, and said supplying of the first instance's actual value is in accordance with the value prediction qualifier.

35. The method of claim 34 further comprising:

determining if the actual value of the subsequent instance of the read operation matches the supplied indicated value;

if the subsequent instance's actual value and the supplied value match, committing the subsequent instance of the read operation; and

updating the value prediction qualifier in accordance with said determining.

36. The method of claim 35, wherein said updating the value prediction qualifier comprises increasing the value prediction qualifier if the subsequent instance's actual value is determined to match the supplied value and decreasing the value prediction qualifier if the subsequent instance's actual value is determined not to match the supplied value.

37. The method of claim 25 embodied as a computer program product encoded on one or more machine-readable media.

38. A method comprising:

recording actual values of prior instances of read operations that miss in low-latency memory; and

supplying the actual values of the prior instances of the read operations to respective ones of subsequent instances of the read operations as predicted values, wherein the subsequent instances of the read operations also miss in the low-latency memory.

39. The method of claim 38, wherein the low-latency memory includes one or more of L1 cache and L2 cache.

40. The method of claim 38 further comprising:

preserving execution state prior to speculative execution of the prior read operations instances with the supplied values; and

recovering execution state when predicted values are determined to be mis-predicted values.

41. The method of claim 40, wherein preserving execution state comprises buffering results of instances of operations that are dependent on value predicted instances of the read operations, at least until the predicted values are verified.

42. The method of claim 40, wherein preserving execution state comprises checkpointing register state.

43. The method of claim 38 further comprising verifying predicted values as accurately predicted values.

44. The method of claim 38, wherein the actual values are recorded in a missing read operations value prediction encoding.

45. The method of claim 44 further comprising indicating the read operations in the missing read operations value prediction encoding.

46. The method of claim 45 further comprising indicating, in the missing read operations value prediction encoding, value prediction qualifiers for the indicated read operations.

47. The method of claim 46, wherein the value prediction qualifiers include one or more of confidence values and strength values.

48. The method of claim 45, wherein the read operations are indicated with one or more of their program counter high order bits, program counter low order bits, program counter, and history information.

49. The method of claim 48, wherein one or more of the read operations indicators are hashed individually or together.

50. A processing unit comprising:

memory;

a missing read operations value prediction encoding to host predicted values for instances of read operations that miss in the memory; and

a memory operations unit coupled with the memory, the memory operations unit including, a missing read operation detection logic to detect instances of read operations that miss in the memory and to indicate those instances of read operations that miss in the memory.

51. The processing unit of claim 50, wherein the memory operations unit further comprises a missing read operation value predictor logic to utilize the missing read operations value prediction encoding to value predict for read operations instances indicated by the missing read operation detection logic.

52. The processing unit of claim 50, wherein the memory includes low-latency memory.

53. The processing unit of claim 52, wherein the low-latency memory includes one or more of L1 cache and L2 cache.

54. The processing unit of claim 50, wherein the memory operations unit includes a hardware structure to host the missing read operations value prediction encoding.

55. The processing unit of claim 50, wherein a region of the memory is marked during initialization of the processing unit to host the missing read operations value prediction encoding.

56. The processing unit of claim 55, wherein, during initialization of the processing unit, the marked region of the memory is marked to prevent entries of the

missing read operations value prediction encoding from migrating to a second memory.

57. The processing unit of claim 56, wherein the second memory includes L1 cache.

58. The processing unit of claim 55 further comprising the missing read operation detection logic to cause issuance of first traps coincident with the missing read operation detection logic detecting a read operation instance missing in the memory, wherein the traps are issued to a trap handler.

59. The processing unit of claim 58, wherein the trap handler supplies predicted values to the memory operations unit for missing instances of read operations from the missing read operations value prediction encoding.

60. The processing unit of claim 59 further comprising the processing unit to generate second traps coincident with arrival of actual values for respective missing instances of read operations, wherein the trap handler updates the missing read operations value prediction encoding in accordance with the second traps.

61. The processing unit of claim 55, wherein the processing unit invokes a value predictor finite state machine that performs value prediction with the missing read operations value prediction encoding.

62. The processing unit of claim 50, wherein the memory operations unit includes a load store queue or a memory disambiguation buffer.

63. The processing unit of claim 50 further comprising an operations retirement unit coupled with the memory operations unit, the operations retirement unit to cause installation of entries in the missing read operations value prediction encoding for missing instances of read operations.

64. An apparatus comprising:

memory; and

means for detecting and indicating read operations instances that miss in the memory and value predicting for respective ones of subsequent instances of the read operations that also miss in the memory.

65. The apparatus of claim 64, wherein the memory includes low-latency memory.

66. The apparatus of claim 65, wherein the low-latency memory includes one or more of L1 cache and L2 cache.

67. The apparatus of claim 64 further comprising means for preserving and recovering execution state in accordance with whether value prediction are accurate.

68. A system comprising:

a first memory and second memory; and

a processing unit coupled with the first memory, the processing unit including,

a missing read operations value prediction encoding to host predicted values for instances of read operations that miss in the second memory

a missing read operation detection unit coupled with the second memory, the missing read operations detection unit to indicate instances of read operations that miss in the second memory.

69. The system of claim 68, wherein the processing unit includes the second memory.

70. The system of claim 68, wherein accesses to the first memory by the processing unit incurs latency.

71. The system of claim 68, wherein the processing unit includes a memory operations unit that includes the missing read operation detection unit.

72. The system of claim 71, wherein the memory operations unit includes a load store queue or a memory disambiguation buffer.

73. The system of claim 71, wherein the memory operations unit includes a structure to host the missing read operations value prediction encoding.

74. The system of claim 73, wherein the structure includes a content addressable memory.

75. The system of claim 68, wherein the first memory includes one or more of L3 cache, random access memory, flash memory, erasable programmable memory, and read-only memory.

76. The system of claim 68, wherein the processing unit includes a missing read operation value predictor logic to utilize the missing read operations value prediction encoding to value predict for read operations instances indicated by the missing read operation detection logic.

77. The system of claim 68, wherein the missing read operations value prediction encoding is instantiable in the second memory.

78. The system of claim 77, wherein the missing read operations encoding can be shared among multiple cores of the processing unit.

79. The system of claim 78,

wherein a second missing read operations encoding can also be shared among the multiple cores, and

wherein the missing read operations encoding and the second missing read operations encoding are instantiated for different applications.

80. The system of claim 77, wherein the second set of memory includes L2 cache and L1 cache, wherein the missing read operation value predictor is instantiable in the L2 cache, but entries thereof are prevented from migrating to the L1 cache.

81. The system of claim 68 further comprising a bus that couples the first memory with the processing unit.

82. The system of claim 68, wherein the processing unit includes a first store to host instances of write operations dependent on value predicted instances of read operations and a second store to host results of the instances of dependent write operations at least until verification of corresponding value predictions.

83. A computer program product encoded in one or more machine-readable media, the computer program product comprising:

a first sequence of instructions executable to select an entry in a missing read operations value prediction encoding that corresponds to a read operation instance that misses in low-latency memory, and to supply a predicted value indicated in the selected entry for the missing read operation instance, wherein the selection is coincident with detection of the read operation instance missing in low-latency memory; and

a second sequence of instructions executable to update the missing read operations value prediction encoding to reflect accuracy of value predictions for missing instances of read operations.

84. The computer program product of claim 83, wherein the missing read operations value prediction encoding is instantiable in the low-latency memory.

85. The computer program product of claim 84, further comprising a third sequence of instructions executable to prevent migration of the entries of the missing read operations value prediction encoding from the low-latency memory to a second memory.

86. The computer program product of claim 85, wherein the low-latency memory includes L2 cache and the second memory includes L1 cache.

87. The computer program product of claim 83, further comprising trap handler code that includes the first and second sequences of instructions, wherein a first set of the traps at least indicate missing instances of read operations, and a second set of the traps at least indicate missing instances of read operations and actual values thereof.

88. The computer program product of claim 83 further comprising a value predictor finite state machine code that includes the first sequence of instructions.

89. The computer program product of claim 88, wherein the value predictor finite state machine code receives indications of missing instances of read operations and constructs addresses therefrom to access the missing read operations value prediction encoding.

90. The computer program product of claim 89, wherein the value predictor finite state machine contains a base register also used in constructing the addresses.

91. The computer program product of claim 89 further comprising trap handler code that includes the second sequence of instructions, wherein traps handled by the trap handler at least indicate missing instances of read operations.

92. The computer program product of claim 91, wherein the trap handler accesses the missing read operations value prediction encoding with addresses constructed from a base address and read operations identifying information.

93. The computer program product of claim 83, wherein the first sequence of instructions to select the entry in the missing read operations value prediction encoding comprises the first sequence of instructions to,

access the entry in the missing read operations value prediction encoding with an index; and

determine that the accessed entry corresponds to the missing read operation instance.

94. The computer program product of claim 93, wherein the index is at least a part of the read operations static identifier.

95. The computer program product of claim 94, wherein the static identifier includes the read operation's program counter.

96. The computer program product of claim 93 further comprising constructing the index.

97. The computer program product of claim 96, wherein said constructing the index comprises hashing the read operation's static identifier.

98. The computer program product of claim 96, wherein said constructing the index comprises hashing the read operation's static identifier with history of the read operation.

99. A missing read operation value prediction structure encoded in one or more machine-readable media, the missing read operation value prediction structure comprising:

an index field to indicate an index;

a missing read operation field to indicate a read operation that misses in low-latency memory;

a predicted value field to indicate a predicted value for instances of a read operation indicated in the missing read operation field; and

a value prediction qualifier field to indicate a value prediction qualifier, wherein a predicted value indicated in the predicted value field is supplied to an instance of a read operation indicated in the missing read operation field in accordance with a value prediction qualifier indicated in the value prediction qualifier field.

100. The missing read operation value predictor structure of claim 99, wherein the index includes one or more of a program counter, low-order bits of a program counter, high-order bits of a program counter, and history information.

101. The missing read operation value predictor structure of claim 99, wherein the indication of the read operation includes one or more of at least a part of a program counter of the read operation, history information of the program counter, a hash of at least a part of the program counter, a hash of the history information, and a hash of the program counter and the history information.

102. The missing read operation value predictor structure of claim 99, wherein the value prediction qualifier includes one or more of confidence, strength, and counter.